IN THE CLAIMS:

Claims 1-12 canceled.

13. (Currently amended) A method for programmably allocating ~~system~~ resources to accommodate I/O transactions at I/O ports of a multiprocessor computer system comprising ~~the steps of~~:

~~determining the number and types of transactions anticipated at a port,~~

D4

determining the number ~~and types~~ of devices being serviced via the ports,

identifying at least one assembly~~ies~~ for hot swapping,

~~copying the states and status of those assemblies,~~

~~copying the states and status of the memory systems associated with those assemblies,~~

~~copying the contents of control registers associated with those assemblies,~~

copying the contents of cache memories associated with the at least one identified ~~those~~ assembly~~ies~~,

~~determining the operating speeds and latency for transactions at the port,~~

~~determining priority of transactions at the port,~~

~~in addition to the above,~~ setting ~~other~~ criteria for transactions at the port with respect to the number ~~and types~~ of ~~transactions and~~ devices, and

with respect to the numbers ~~and types~~ of ~~transactions and~~ devices at the ports, assigning ~~system~~ resources to the ports.

14. (Currently amended) The method as defined in claim 13 wherein ~~the step of~~ assigning system resources to the ports comprises ~~includes~~ at least one of assigning control registers to the ports, assigning direct memory access engines to the ports, assigning cache memory to the ports and assigning priorities among the transactions at the ports.

15. (Currently amended) A system for programmably allocating ~~system~~ resources to accommodate I/O transactions at I/O ports of a multiprocessor computer system, the system comprising:

D4

~~means for determining the number and types of transactions anticipated at a port,~~

means for determining the number ~~and types~~ of devices being serviced via a ~~the~~ port,

at least one assembly~~ies~~ identified for hot swapping,

~~means for copying the states and status of those assemblies,~~

~~means for copying the states and status of the memory systems associated with those assemblies,~~

~~means for control the contents of registers associated with those assemblies,~~

means for copying the contents of cache memories associated with the at least one identified ~~those~~ assembly~~ies~~,

~~means for determining the operating speeds and latency for transactions at the port,~~

~~means for determining priority of transactions at the port,~~

~~in addition to the above,~~ means for setting ~~other~~ criteria for transactions at the port with respect to the number ~~and types~~ of ~~transactions and~~ devices, and

~~with respect to the criteria, numbers and types of transactions and devices at the ports,~~ means, responsive to the criteria, for assigning ~~system~~ resources to the ports.

16. (Currently amended) The system as defined in claim 15 wherein the ~~system~~ resources assigned to the ports comprises ~~includes~~ at least one of ~~control registers,~~

direct memory access (DMA) engines,

cache memory, and

D4

means for ~~foe~~ assigning priorities among the transactions at the ports.

17 (New) The method as defined in claim 13 further comprising determining the number and types of transactions anticipated at the ports, wherein the assignment of resources is further with respect to the numbers and types of transactions at the ports.

18. (New) The method as defined in claim 13 wherein the at least one identified assembly has a memory system, and the method further comprises copying the states and status of the memory systems associated with at least one identified assembly.

19. (New) The system as defined in claim 15 further comprising means for determining the number and types of transactions anticipated at the ports, wherein the criteria further accounts for the anticipated number and types of transactions.

20. (New) The system as defined in claim 15 wherein the at least one identified assembly has a memory system, and the system further comprises means for copying the states and status of the memory systems associated with the at least one identified assembly.

21. (New) A method for programmably allocating resources for processing Input/Output (I/O) transactions at a plurality of I/O ports of an I/O bridge, the method comprising:

identifying the number of I/O devices being serviced by at least one I/O port;

setting criteria for the transactions at the at least one I/O port with respect to the number of I/O devices being serviced by the port; and

D4

assigning the resources to the at least one I/O port in response to the criteria.

22. (New) The method of claim 21 wherein the assigning comprises assigning a plurality of direct memory access (DMA) engines for use in processing I/O transactions.

23. (New) The method of claim 22 wherein assigning comprises apportioning a selected number of DMA engines to process a given transaction at a particular I/O port.

24. (New) The method of claim 22 wherein assigning comprises apportioning at least one DMA engine to process at least one transaction at a port.

25. (New) The method of claim 22 wherein assigning comprises apportioning one DMA engine to process a given transaction at a port identified as servicing multiple I/O devices.

26. (New) The method of claim 21 wherein assigning comprises assigning at least one miss address file (MAF) value for processing I/O transactions.

27. (New) The method of claim 21 wherein assigning comprises assigning a plurality of miss address file (MAF) values for processing I/O transactions.

28. (New) The method of claim 27 further comprising reducing the assigned number of MAF values.

29. (New) The method of claim 21 wherein

the I/O bridge is configured to utilize a plurality of virtual channels to communicate with at least one processors of a multiprocessor computer system, and

the resources include flow control credits associated with each of the plurality of virtual channels.

30. (New) The method of claim 29 wherein assigning comprises setting the number of flow control credits associated with each virtual channel.

31. (New) The method of claim 21 wherein

the I/O bridge comprises at least one control register, the at least one control register having a plurality of fields, and at least one field of the control register being associated with a corresponding resource, and

the method further comprises writing to a selected field of the at least one control register so as to modify the assignment of resources.

32. (New) An Input/Output (I/O) bridge for use in a computer system having a plurality of processors, the I/O bridge comprising:

a plurality of I/O ports, each I/O port configured to communicate with at least one I/O device that generates or receives transactions;

resources for use in servicing the transactions of the I/O devices; and

programmable logic configured and arranged to assign the resources among the I/O ports in response to the number of I/O devices with which the I/O ports are communicating.

33. (New) The I/O bridge of claim 32 wherein

the resources comprise at least one direct memory access (DMA) engine configured to process the transactions, and

the programmable logic apportions the at least one of DMA engine to process at least one transaction at a given I/O port in response to the number of I/O devices coupled to the given I/O port.

D4

34. (New) The I/O bridge of claim 32 wherein

the resources include a plurality of miss address file (MAF) values for use in requesting information from the computer system, and

the programmable logic sets the number of available MAF values.

35. (New) The I/O bridge of claim 32 wherein

the I/O bridge communicates with the computer system through a plurality of virtual channels,

the resources include a plurality of flow control credits associated with the virtual channels, and

the programmable logic assigns a number of flow control credits to each virtual channel.

36. (New) the I/O bridge of claim 35 wherein the virtual channels comprise a Request channel, a Read I/O channel, and a Write I/O channel.

37. (New) The I/O bridge of claim 33 further comprising at least one cache for storing information, wherein, to hot-swap an assembly of the computer system, the programmable logic is configured to

disable the at least one DMA engine, and

flush the information from the at least one cache.

D4

38. (New) The I/O bridge of claim 37 wherein the at least one cache is one of a write cache, a read cache and a translation look-aside buffer (TLB).

39. (New) The I/O bridge of claim 37 wherein the assembly is a processor.

40. (New) The I/O bridge of claim 33 wherein

the programmable logic comprises at least one control register associated with each I/O port, and

the at least one control register has a first field for apportioning the at least one DMA engine.

41. (New) The I/O bridge of claim 32 wherein the programmable logic re-assigns resources among the I/O ports dynamically while the I/O bridge continues to operate.